MODULE DATASHEET

PN7160 / PN7161 NFC RFID Module - I2C Version

Module Datasheet

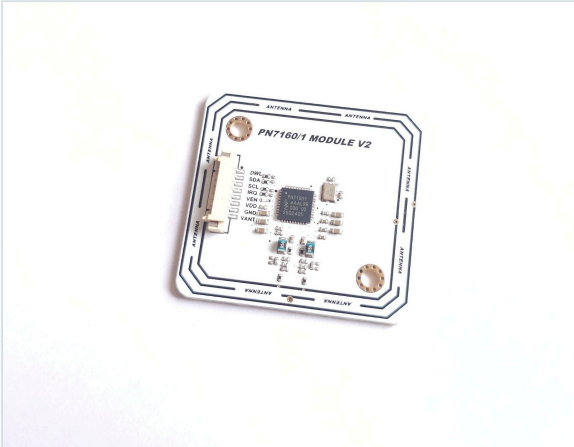
Updated 2026-07-18

Host Interface
I2C with IRQ, VEN, DWL_REQ

RF Band
13.56 MHz NFC / RFID

Logic Supply
3.3 V typical, optional 1.8 V

RF Supply
VANT 5.0 V typical



Product photo - PN7160/PN7161 I2C module family

Variants
PN7160 and PN7161 I2C module family

Applications
Embedded NFC, Raspberry Pi, ESP32, Linux, Android

Document
Version V1.1
Updated 2026-07-18

1. Overview

The ELECHOUSE PN7160 / PN7161 NFC RFID Module - I2C Version is a compact NFC controller module with an on-board PCB antenna and I2C host interface. The PN7160 and PN7161 I2C products use the same module hardware design; the populated NFC controller IC is different.

- PN7160 version: PN7160A controller, suitable for Linux, Android, Raspberry Pi, ESP32, and embedded NFC applications where Apple ECP is not required.
- PN7161 version: PN7161 controller, same hardware design with Apple ECP capability for Apple-related reader projects.
- Standard host interface: I2C with IRQ, VEN, and DWL_REQ control pins.
- On-board tuned PCB antenna and RF matching network.
- Two external supply inputs: VDD for host-interface logic and VANT for antenna/RF transmitter supply.

2. Product Variants and Ordering Information

Variant	SKU	Populated IC	Apple ECP Hardware Support	Notes
PN7160 NFC RFID Module	NFC_PN7160_I2C	NXP PN7160A	No	Lower-cost default choice when Apple ECP is not required.
PN7161 NFC RFID Module	NFC_PN7161_I2C	NXP PN7161	Yes - hardware support only	Use when Apple ECP-related hardware support may be required. Apple Wallet / Apple VAS authorization, certification, and software integration are handled by the customer.

3. Module Specifications

3.1 Module Specifications

Parameter	Value / Recommendation
Host interface	I2C with IRQ, VEN, and DWL_REQ control pins.
I2C interface speed	Supports Standard-mode up to 100 kHz, Fast-mode up to 400 kHz, and High-speed mode up to 3.4 MHz. Fast-mode Plus (1 MHz) is not supported.
Connector / cable	Board connector: MX1.25 8P / 1.25 mm pitch vertical SMT header, 8-pin. Compatible reference: Molex PicoBlade™ 53398-0871 or equivalent. Matching cable / wire harness: JST1.25 8P / 8-pin matching housing. Compatible reference: Molex PicoBlade™ 51021-0800 or equivalent with pre-crimped terminal wires.
Default I2C address	7-bit 0x28; 8-bit write/read 0x50 / 0x51.
I2C address range	0x28 to 0x2B via ADR0 / ADR1 configuration.

Parameter	Value / Recommendation
ADR0 / ADR1 address setting	When 100 kΩ pulldown resistors are present, unpopulated ADRx = 0 and populated/soldered ADRx = 1. Recommended 0402 address-setting resistor: 10 kΩ, or 0 Ω jumper resistor; common for 1.8 V and 3.3 V systems.
I2C pull-up resistors	Recommended 2.2 kΩ pull-ups for both 1.8 V and 3.3 V logic levels.
VDD	Standard recommendation: 3.0-3.6 V, typ. 3.3 V. Optional 1.65-1.95 V operation, typ. 1.8 V, is supported for 1.8 V host-interface systems.
VDD optional 1.8 V mode	The module supports VDD(PAD) operation at 1.65-1.95 V. I2C signals (SDA/SCL), control inputs (VEN/DWL_REQ), and IRQ operate at the selected VDD logic level. Use 1.8 V I/O and 1.8 V I2C pull-ups when VDD is 1.8 V. The onboard PWR LED may be very dim or off at 1.8 V; this is normal and does not affect operation.
VANT	Recommended: 4.75-5.25 V, typ. 5.0 V.
VANT absolute maximum	6.0 V max recommended at module pin.
Operating temperature	-30°C to +85°C.
Storage temperature	-40°C to +85°C. Keep +85°C as the module-level limit because connector plastics, LEDs, labels, and standard assembly materials are typically rated to +85°C.
Operating humidity	20% to 90% RH, non-condensing.
Storage humidity	5% to 90% RH, non-condensing. Store in ESD shielding bags in a dry, temperature-controlled environment.
Crystal	27.12 MHz, 3225 package, 10 pF load.
Antenna	On-board PCB antenna with tuned RF matching network.
PCB dimensions	42.70 mm × 40.10 mm.
PCB thickness	1.6 mm.
Mounting holes	2 pcs, Ø 3.048 mm.
Compliance	CE and RoHS certified. Full laboratory test reports and certificate packages are available for download from the ELECHOUSE website; see Section 9.

3.2 Typical Test Results

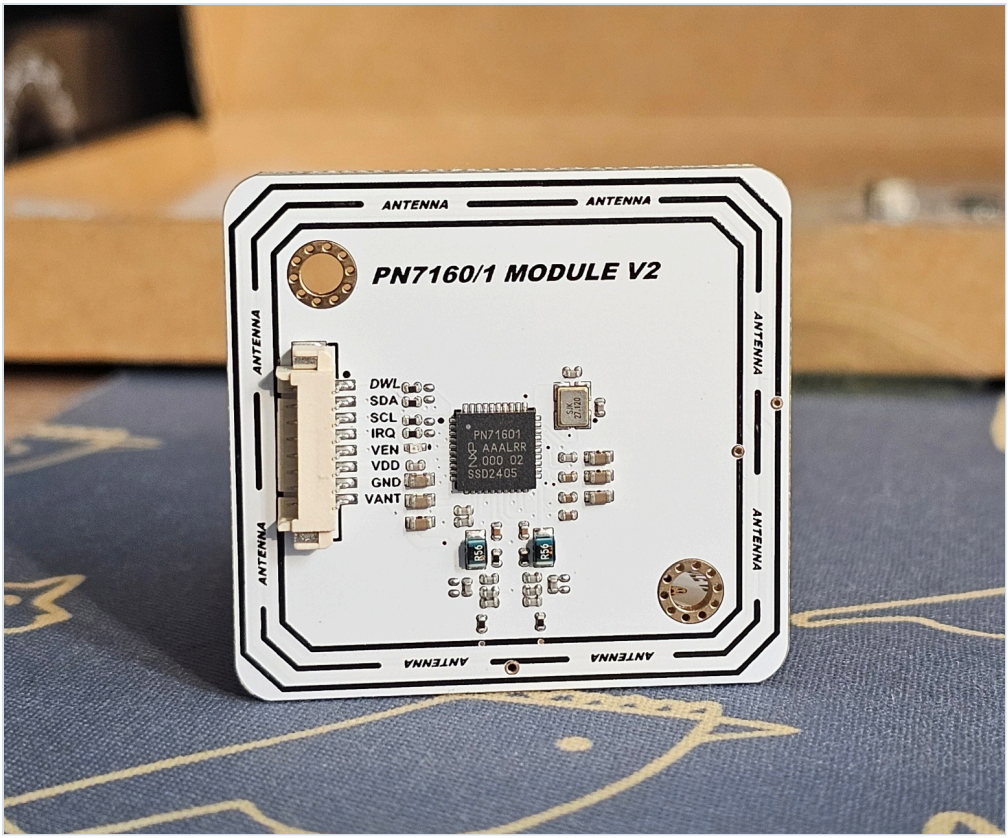
Item	Typical observed result	Condition / Limitation
Power consumption	Typical observed module power at VDD=3.3 V and VANT=5.0 V: sleep approx. 1.15 mW, normal card read approx. 332.40 mW, and maximum read stress mean approx. 333.07 mW. See Section 5.1 for VANT and VDD current values.	Measured at VDD=3.3 V and VANT=5.0 V with the external host/controller current excluded. Values are typical observed reference data only; observed current maxima are not guaranteed maximum ratings.
Read range	See Section 7.1. Typical observed values in the supplied PN7160 I2C card/tag table are approx. 5.5-14 cm depending on card/tag type.	Observed at VDD=3.3 V and VANT=5.0 V, in a metal-free environment and without metal anti-magnetic/shielding sticker. These values are not guaranteed minimum read distances and may vary between modules, cards/tags, orientations, and installation environments.

3.3 Notes / Conditions

Item	Note / Condition
Observed values	Power-consumption and read-range data are typical observed reference values. Neither is a production test limit unless explicitly defined and agreed for a specific project.
Power measurement scope	PN7160 module only; external host/controller current is excluded. Values are observed at VDD=3.3 V and VANT=5.0 V.
Transient behavior	The table reports phase-average module power and observed current maxima for tested operating states. System power-supply margin and short transient behavior should be validated in the final product design.
Read-range variability	Read range may vary between modules, cards/tags, card orientation, nearby metal, enclosure design, cable routing, ferrite absorber sheet, and other installation conditions. No fixed statistical percentage is specified in this datasheet.
PN7160 / PN7161 RF performance	PN7160 and PN7161 module versions use the same module RF front-end and antenna layout; read-range performance is expected to be similar. If PN7161 read range is critical for a project, validate with PN7161 samples in the final installation.
Apple ECP / Apple Wallet / Apple VAS	PN7161 provides hardware support related to Apple ECP reader projects. Apple Wallet / Apple VAS authorization, certification, and application-level software integration remain the customer’s responsibility.
Metal and ferrite absorber sheet	For metal vertically behind the read-card area, ≥50 mm clearance is recommended for best performance. If <50 mm is unavoidable, use a ferrite absorber sheet; typical absorber sheet: 0.1-0.3 mm thickness, μ′ 60-150 at 13.56 MHz.
Card-specific tuning	Card-specific matching/tuning is a customization service, normally used only for demanding installations where the card/tag type is fixed.

4. Connector Pinout

The module uses an MX1.25 8P board connector. The matching cable / wire harness is JST1.25 8P.



Connector orientation reference supplied by ELECHOUSE

Pin	Signal	Direction	Description / Notes
1	DWL / DWL_REQ	Input	Download request / firmware mode control. 10 kΩ pulldown to GND; default low for normal boot.
2	SDA	I/O	I2C data. No fixed on-board pull-up shown; host side must provide pull-up to the selected VDD logic level. Recommended pull-up: 2.2 kΩ for both 1.8 V and 3.3 V.
3	SCL	Input	I2C clock. No fixed on-board pull-up shown; host side must provide pull-up to the selected VDD logic level. Recommended pull-up: 2.2 kΩ for both 1.8 V and 3.3 V.
4	IRQ	Output	Interrupt output to host. Logic level follows VDD(PAD).
5	VEN	Input	Enable / reset control from host. Logic level follows VDD(PAD).
6	VDD	Power	Logic / host-interface supply. Standard recommendation 3.3 V; 1.8 V operation is supported when host I/O and pull-ups also use 1.8 V.
7	GND	Power	Ground reference.
8	VANT	Power	Antenna / RF transmitter supply. Use 5.0 V typ.; 3.3 V is not supported for reliable card detection.

5. Power Supply Requirements

Supply	Recommended Operating Condition	Absolute Maximum / Caution
VDD	3.0-3.6 V, typ. 3.3 V for standard use. Optional 1.65-1.95 V, typ. 1.8 V, for direct connection to 1.8 V MCUs. When using 1.8 V, tie host-side I2C pull-ups to the 1.8 V rail and use 1.8 V host I/O for SDA, SCL, IRQ, VEN, and DWL_REQ.	VDD(PAD) absolute max 4.2 V per NXP. Do not drive 3.3 V GPIO into the module when VDD is 1.8 V. The onboard PWR LED (D1) may be very dim or off at 1.8 V; this is expected and does not affect chip operation.

Supply	Recommended Operating Condition	Absolute Maximum / Caution
VANT	4.75-5.25 V, typ. 5.0 V.	Recommended module absolute max 6.0 V. VANT below 5 V is not guaranteed for reader/writer operation; 3.3 V VANT failed card detection in ELECHOUSE testing.
GND	Common ground between module and host.	Required for all signal and power connections.

5.1 Power Consumption

Typical observed PN7160 module current and power at VDD=3.3 V and VANT=5.0 V. The external host/controller current is excluded. Values below are reference observations only, not production test limits or guaranteed maxima.

Operating state	VANT current at 5.0 V (mean / observed max)	VDD current at 3.3 V (mean / observed max)	Typical observed module power	Notes
Sleep, VEN low	0.0098 / 0.018 mA	0.333 / 0.338 mA	1.15 mW	Lowest tested state; VEN held low.
Normal card read, 500 ms	66.58 / 66.71 mA	0.325 / 0.384 mA	332.40 mW	Representative card-read workload.
Maximum read stress, 200 ms	66.71 / 66.84 mA	0.326 / 0.381 mA	333.07 mW	Highest tested active workload mean.
Return to sleep	0.0099 / 0.019 mA	0.335 / 0.339 mA	1.15 mW	Final VEN-low state after active phases.

5.2 Simplified Functional Block Diagram

The simplified functional path below summarizes the module-level connections. The public schematic PDF is listed in Section 9.

Block / Interface	Module-level function
Host interface supply	VDD(PAD) / VDD pin provides the 1.8 V or 3.3 V host I/O domain. SDA and SCL require host-side pull-ups; IRQ, VEN, and DWL_REQ logic levels follow VDD.
I2C and control pins	SDA, SCL, IRQ, VEN, and DWL_REQ connect the host MCU or Linux controller to the PN7160/PN7161. DWL_REQ has an onboard 10 kΩ pulldown for normal boot.
RF transmitter supply	VANT provides the 5 V RF transmitter / antenna supply. VDD and VANT are separate external rails because R25 is DNP in the production module.
RF path	PN7160/PN7161 RF output → EMC filter and matching network → on-board PCB loop antenna.

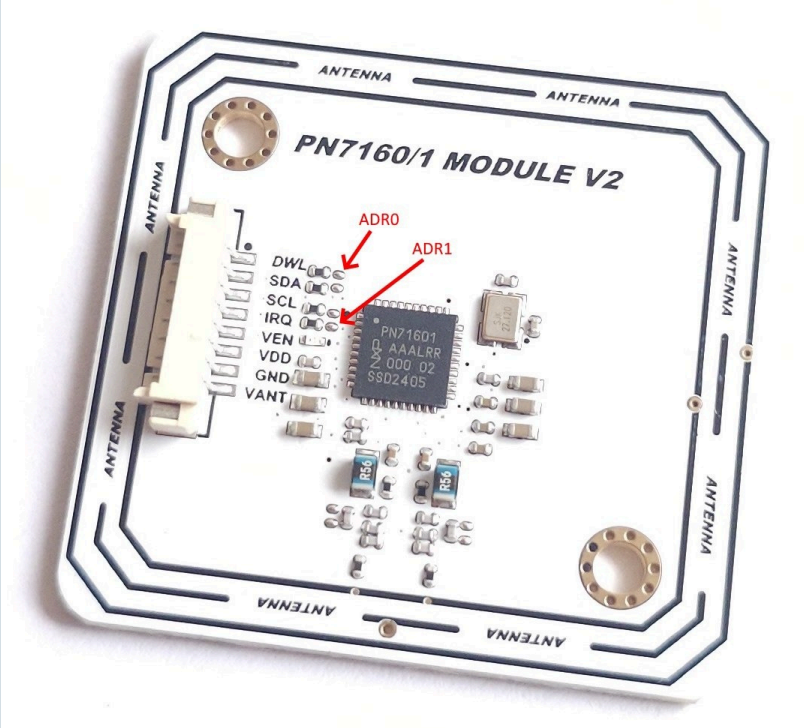
6. I2C Interface and Addressing

- Default 7-bit I2C address: 0x28.
- 8-bit write/read addresses: 0x50 / 0x51.
- The module does not show fixed on-board SDA/SCL pull-up resistors in the supplied netlist/schematic. Host-side pull-ups are required; recommended value is 2.2 kΩ.
- Pull-up voltage must match VDD logic level (3.3 V for standard use, 1.8 V only when using 1.8 V VDD/PAD mode).
- Use 2.2 kΩ pull-up resistors for both 1.8 V and 3.3 V I2C pull-up rails unless the host bus design requires a different value after validation.

- Supported I2C bus modes: Standard-mode (up to 100 kHz), Fast-mode (up to 400 kHz), and High-speed mode (up to 3.4 MHz). Fast-mode Plus (1 MHz) is not supported.

6.1 ADR0 / ADR1 Soldering Address Setting

ADR0 and ADR1 select the I2C physical address. When the 100 kΩ pulldown resistors are present, the default unpopulated state is logic 0. Soldering/populating the ADR0 or ADR1 option position sets the corresponding bit to logic 1.



ADR0 / ADR1 soldering positions for I2C address selection

Item	Recommendation / Meaning
Recommended ADR0 / ADR1 soldering resistor	0402 resistor, 10 kΩ recommended; 0 Ω jumper resistor may also be used.
Applicable logic systems	The same recommendation applies to both 1.8 V and 3.3 V systems.
Address-state definition	0 = not soldered / default pulled down by 100 kΩ; 1 = soldered/populated address-setting resistor.

ADR0	ADR1	7-bit I2C Physical Address	8-bit Write	8-bit Read
0	0	0x28 (default)	0x50	0x51
1	0	0x29	0x52	0x53
0	1	0x2A	0x54	0x55
1	1	0x2B	0x56	0x57

6.2 Power-up, Reset, and Control Pin Timing

Item	Requirement / Behavior
Hardware reset via VEN	Hold VEN low for ≥10 µs to reset the module.
Boot-up delay	After pulling VEN high with stable VANT and VDD, wait at least 2.5 ms before initiating the first I2C communication.

Item	Requirement / Behavior
IRQ behavior	IRQ is an active-high digital output. It rises to the VDD logic level when NCI data is pending and returns low after the host reads the data packet over I2C.
Normal boot	Keep DWL_REQ low during boot. The module's onboard 10 kΩ pulldown keeps DWL_REQ low by default.
Firmware download boot	Pull DWL_REQ high before pulling VEN high. DWL_REQ high level is referenced to the VDD logic level.

7. NFC / RF Capabilities

Item	Description
Operating frequency	13.56 MHz NFC / RFID band
Supported modes	Reader/Writer, Peer-to-Peer, Card Emulation
Protocols / technologies	ISO/IEC 14443A/B, ISO/IEC 15693, FeliCa, MIFARE, NFC Forum Type 1-5 tags. Final supported features may depend on host software stack and integration.
Antenna	On-board PCB antenna with tuned matching network.
Typical observed read range	Approx. 5.5-14 cm in the supplied PN7160 I2C read-range test table at VDD=3.3 V and VANT=5.0 V. Test condition: no surrounding metal and no metal anti-magnetic/shielding sticker. Actual range depends on tag/card type, antenna size, orientation, module variation, and installation environment. Reference observation only; not a guaranteed minimum.
Card-specific optimization	For different cards/tags, the module can be individually debugged and matched/tuned to optimize performance for the selected card type. This is a custom service, usually only needed when the application environment is demanding and the card/tag type is fixed.

7.1 Read Range Test Data

The following table is transcribed from the ELECHOUSE supplied read-range screenshot. Test condition shown in the screenshot: PN7160 I2C module, VANT=5 V, VDD=3.3 V. ELECHOUSE test condition: no surrounding metal and without a metal anti-magnetic/shielding sticker. Values are typical observed reference results only; they are not production test limits and not guaranteed minimum read distances.

7.1.1 Read Range Test Method and Notes

Item	Definition / Note
Test method	Continuous polling / reading loop. A read is considered successful when the card UID / card number is detected and decoded.
PN7160 / PN7161 expected RF similarity	PN7160 and PN7161 module versions use the same module RF front-end and antenna layout, so read-range performance is expected to be similar. If PN7161 read range is critical, validate using PN7161 samples in the final installation.
Tolerance disclaimer	Read-range values are typical reference observations measured in a metal-free environment without metal anti-magnetic/shielding sticker. Actual read range may vary between modules, cards/tags, orientations, production tolerances, enclosures, nearby metal, cable routing, and other installation environments.

Tag / Model	Standard	Protocol	Chip / Variant	Size (cm)	Typical observed read range (cm) / not guaranteed minimum
NFC Type 1 Tag	ISO 14443A	T1T (0x1)	Topaz 512	8.5 × 5.4	10.5

Tag / Model	Standard	Protocol	Chip / Variant	Size (cm)	Typical observed read range (cm) / not guaranteed minimum
NFC Type 2 Tag	ISO 14443A	T2T (0x2)	MIFARE Ultralight C	8.5 × 5.4	5.5
NFC Type 2 Tag (Ultralight AES)	ISO 14443A	T2T (0x2)	Ultralight AES	8.5 × 5.4	10.5
NFC Type 2 Tag (Ultralight EV1)	ISO 14443A	T2T (0x2)	Ultralight EV1	8.5 × 5.4	10.5
NFC Type 2 Tag (NTAG213)	ISO 14443A	T2T (0x2)	NTAG213	8.5 × 5.4	10.4
NFC Type 2 Tag (NTAG215)	ISO 14443A	T2T (0x2)	NTAG215	8.5 × 5.4	10
NFC Type 2 Tag (NTAG216)	ISO 14443A	T2T (0x2)	NTAG216	8.5 × 5.4	10.5
NFC Type 3 Tag	FeliCa / NFC-F	T3T / FeliCa (0x3)	FeliCa Lite-S RC-S966	8.5 × 5.4	9
NFC Type 4 Tag (DESFire 8K)	ISO 14443A	ISO-DEP / Type 4 (0x4)	MIFARE DESFire 8K	8.5 × 5.4	7
NFC Type 4 Tag (NTAG424 DNA)	ISO 14443A	ISO-DEP / Type 4 (0x4)	NTAG424 DNA	8.5 × 5.4	10.7
NFC Type 4 Tag	ISO 14443B	ISO-DEP / Type 4 (0x4)	-	8.5 × 5.4	6.5
NFC Type 5 Tag	ISO 15693	ISO15693 / NFC-V (0x6)	ICODE SLS	8.5 × 5.4	14
NFC Type 5 Tag (ICODE SLIX2)	ISO 15693	ISO15693 / NFC-V (0x6)	ICODE SLIX2	8.5 × 5.4	14
NFC Type 5 Tag (ICODE SLIX)	ISO 15693	ISO15693 / NFC-V (0x6)	ICODE SLIX	8.5 × 5.4	14
MIFARE One S70	ISO 14443A	-	MIFARE One S70	8.5 × 5.4	10.5
MIFARE One S70 compatible card	ISO 14443A	-	MIFARE One S70 compatible card	8.5 × 5.4	8.5
NFC Type 4 Tag	ISO 14443A	ISO-DEP / Type 4 (0x4)	MIFARE DESFire EV1 2K	8.5 × 5.4	7.3

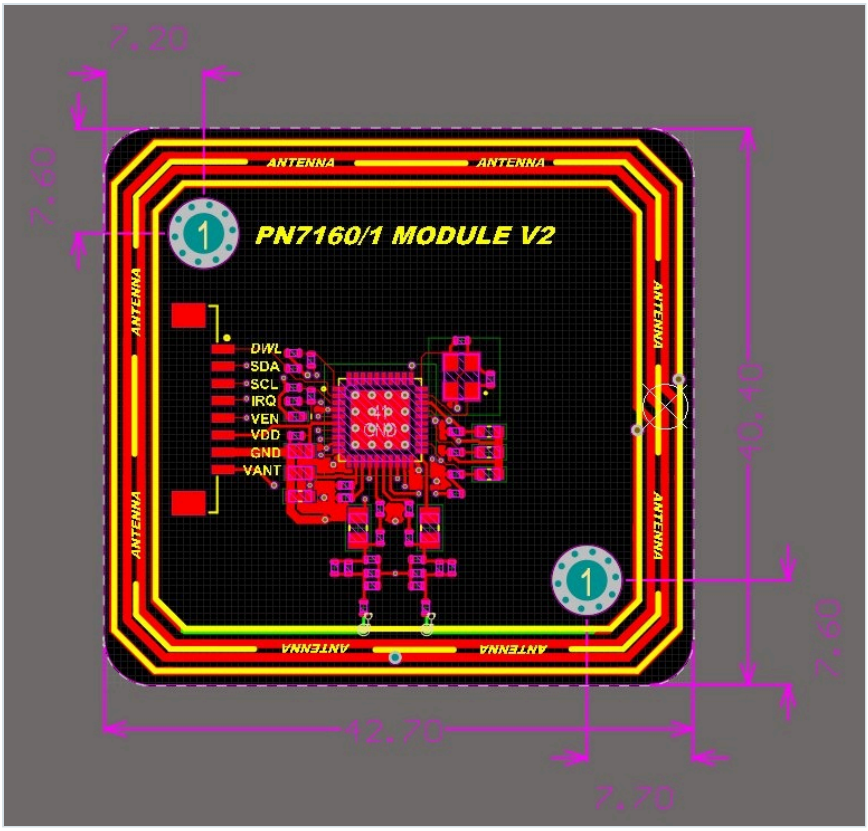
7.2 Card-Specific Matching / Custom Tuning Service

Different card and tag types can have different antenna coupling behavior. For projects that require best performance with a fixed card/tag type, ELECHOUSE can provide card-specific debugging and matching/tuning as a customization service.

- This service is intended to optimize performance for the customer’s selected card/tag type and real installation environment.
- It is typically only required when the application environment is relatively demanding, such as metal nearby, constrained installation space, strict read-distance requirements, or other harsh RF conditions.
- It is most suitable when the card/tag type is fixed. If customers use many different card/tag types, a general-purpose tuning target should be selected instead of optimizing for one specific card.
- Final performance depends on the selected card/tag, installation structure, metal clearance, ferrite absorber sheet, and production tolerance; project-specific validation is recommended.

> Apple ECP note: PN7161 provides hardware support related to Apple ECP reader projects. Apple Wallet / Apple VAS authorization, certification, and application-level software integration remain the customer’s responsibility. ELECHOUSE provides hardware/module support only.

8. Mechanical Information



Mechanical drawing screenshot supplied by ELECHOUSE

Parameter	Value / Status
PCB dimensions	42.70 mm × 40.10 mm
PCB thickness	1.6 mm
Mounting holes	2 pcs, Ø 3.048 mm (0.120 in)
Top-left mounting hole center	7.20 mm from left PCB edge; 7.90 mm from top PCB edge
Bottom-right mounting hole center	7.70 mm from right PCB edge; 7.20 mm from bottom PCB edge
Connector location and orientation	Pinout image available; connector coordinate details can be added if required for carrier-board layout
DXF files	Available as separate downloads; see Section 9 for Dimension, DXF, and 3D file links

8.1 Installation Environment and Metal Clearance

Metal close to the antenna can detune the RF field and reduce read range. For best antenna performance, avoid metal behind the read-card area whenever possible. If metal exists in the vertical direction behind the read-card area, use the following guidance.

Condition	Recommendation / Expected Effect
Metal behind read-card area, distance ≥50 mm	Recommended best-performance installation distance. At this distance, metal has little effect on antenna parameters.

Condition	Recommendation / Expected Effect
Metal behind read-card area, distance <50 mm	If operation at this distance is unavoidable, add a ferrite absorber sheet between the module/read-card area and the metal to reduce antenna detuning. Typical ferrite absorber sheet specification: thickness 0.1-0.3 mm; real permeability μ′ recommended 60-150 at 13.56 MHz.

8.2 Connection Cable Routing Guidelines

Cable routing can affect the 13.56 MHz magnetic field. Follow these guidelines to reduce antenna detuning and read-range loss.

Route the connection cable straight away from the connector and keep it completely outside the PCB antenna boundary / active card-reading zone. If crossover is unavoidable, route the cable harness perpendicular (90°) to the nearest on-board antenna trace to minimize magnetic coupling. Critical warning: Do not route cables in a closed loop or bundle excess wire within the active card-reading zone. A closed loop of wire can behave as a shorted turn, absorbing the 13.56 MHz RF field and drastically reducing read range.

9. Software, Mechanical, Compliance, and Web Resources

Resource	URL
PN7160 product page	https://www.elechouse.com/product/pn7160-nfc-rfid-module/
PN7161 I2C product page	https://www.elechouse.com/product/pn7161-nfc-rfid-module-i2c/
PN7160 documentation	https://www.elechouse.com/docs/pn7160/
PN7161 documentation	https://www.elechouse.com/docs/pn7161/
Quick Guide - PN7160 with Raspberry Pi / Linux I2C	https://www.elechouse.com/wp-content/uploads/2024/06/Quick-Guide-I2C.pdf
Guide - PN7160 with ESP32 in Arduino IDE	https://www.elechouse.com/wp-content/uploads/2024/06/ESP32-and-PN7160-in-Arduino-IDE.pdf
I2C address setting guide	https://www.elechouse.com/wp-content/uploads/2024/06/I2C-address-setting.pdf
PDF schematic	https://www.elechouse.com/wp-content/uploads/2023/11/PN7160_schematic.pdf
Board dimension DXF (ZIP)	https://www.elechouse.com/wp-content/uploads/2024/06/PN7160_I2C_dimension.zip
3D file	https://www.elechouse.com/wp-content/uploads/2023/11/3D_PN7160_V3_2025-12-13.zip
Shared Arduino / ESP32 library	https://github.com/wilson-elechouse/ELECHOUSE_PN7150_PN7160
CE certificate package	https://www.elechouse.com/wp-content/uploads/2024/06/PN716X_CE.zip
RoHS certificate package	https://www.elechouse.com/wp-content/uploads/2024/06/PN7160_1-ROHS.zip

10. Notes

- This file is a module-level datasheet. It does not replace the NXP PN7160/PN7161 chip datasheet.
- Electrical supply ranges are adapted from NXP PN7160/PN7161 Product Data Sheet Rev. 4.0 and ELECHOUSE module test observations.
- VANT is specified as 5 V typical because ELECHOUSE confirmed 3.3 V VANT does not read cards, while 5 V works.
- VDD=1.8 V operation is confirmed to work when host I/O and I2C pull-ups use the same 1.8 V logic level; the specified VDD(PAD) 1.8 V operating range is 1.65-1.95 V, and the PWR LED may be very dim or off at this voltage.
- Recommended I2C pull-up resistor value is 2.2 kΩ for both 1.8 V and 3.3 V pull-up rails.
- Power consumption values are typical observed PN7160 module current and power at VDD=3.3 V and VANT=5.0 V, with the external host/controller current excluded. Normal card read is approx. 332.40 mW; maximum read stress mean is

approx. 333.07 mW; sleep is approx. 1.15 mW. Observed maximum current values are test sample observations only, not guaranteed maximum ratings.

- Read-range values are transcribed from the supplied PN7160 I2C test table screenshot at VDD=3.3 V and VANT=5.0 V; the test condition is no surrounding metal and no metal anti-magnetic/shielding sticker. The test method is continuous polling. Values are typical observed reference data, not guaranteed minimums, and may vary between modules, cards/tags, orientations, and installation environments.
- Installation metal-clearance recommendation: if metal is located vertically behind the read-card area, keep ≥50 mm distance for best performance; at <50 mm, add a ferrite absorber sheet if operation is required. Typical ferrite absorber sheet specification: 0.1-0.3 mm thickness, with real permeability μ′ recommended 60-150 at 13.56 MHz.
- Card-specific debugging and matching/tuning is documented as an ELECHOUSE customization service. It is mainly intended for demanding applications where the selected card/tag type is fixed and best performance with that card/tag is required.
- Storage temperature is deliberately kept at -40°C to +85°C because standard connector plastics, LEDs, adhesive labels, and assembly materials are typically rated to +85°C; exceeding this would require specialized higher-temperature materials.
- Board connector/cable: MX1.25 8P board connector and JST1.25 8P matching cable / wire harness; Molex PicoBlade™ 53398-0871 / 51021-0800 are listed as compatible reference equivalents.
- ADR0/ADR1 address-setting: with 100 kΩ pulldown resistors present, 0 means unpopulated/default pulled down and 1 means the address-setting resistor is soldered; recommended 0402 value is 10 kΩ or 0 Ω, common to 1.8 V and 3.3 V systems.
- I2C timing and control-pin behavior are based on NXP PN7160/PN7161 chip specifications and module-level pin usage: VEN reset low ≥10 μs, boot delay ≥2.5 ms after VEN high, IRQ active-high, and DWL_REQ high before VEN high for firmware download boot.
- Connection cable routing guidance is intended to reduce antenna detuning: keep the cable outside the antenna area when possible, cross at 90° if unavoidable, and avoid closed loops or bundled excess wire in the active read zone.
- The connector pin order follows the ELECHOUSE connector-side orientation image; use the dimension files in Section 9 for carrier-board layout.

11. Revision History

Revision	Date	Description
V1.1	2026-07-18	Updated typical observed module power and VANT/VDD current data for sleep, normal card read, and maximum read stress operating states.
V1.0	2026-06-24	Initial formal version. Separates module specifications, typical observed test results, and notes/conditions; clarifies observed power/read-range values as non-guaranteed reference data; uses conservative PN7160/PN7161 and Apple ECP wording; and keeps the formal resource list limited to product pages, documentation, schematic, dimension files, certificates, and code repository.